or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

FIG. **7** depicts a block diagram of a FET fabrication system **700**, according to various embodiments.

A fabrication controller **710** is communicatively connected to a fabrication apparatus **712**. The fabrication controller **710** may be implemented by various computing devices or computer processes. For example, the computer **600** in FIG. **6** may represent an embodiment of the fabrication controller **710**, according to various embodiments. The fabrication controller **710** may receive inputs from various sources, according to various embodiments. The fabrication apparatus **712** may produce a product **714**, which may be one or more FETs, according to various embodiments.

The descriptions of the various embodiments of the present disclosure have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the described embodiments. The terminology used herein was chosen to explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

What is claimed is:

1. A field-effect transistor (FET) device, comprising:

a silicon germanium on insulator (SGOI) wafer having an nFET region and a pFET region

wherein the nFET region includes a Si layer located above a Si_xGe_{1-x} layer;

wherein the pFET region includes a Si_zGe_{1-z} layer located above a Si_yGe_{1-y} layer; and

wherein the Si_yGe_{1-y} layer has a germanium (Ge) content equal to or greater than the Si_xGe_{1-x} layer, and the Si_zGe_{1-z} layer has a Ge content greater than the Si_yGe_{1-y} layer.

2. The FET device of claim **1**, wherein the SGOI includes:

a silicon (Si) substrate;

a buried oxide (BOX) layer located above the Si substrate, and

a silicon germanium (SiGe) layer located above the BOX layer.

3. The FET device of claim **1**, wherein the Ge content of Si_zGe_{1-z} is greater than the Ge content of Si_yGe_{1-y} by at least 10 atomic percent.

4. The FET device of claim **1**, wherein the Ge content of Si_yGe_{1-y} is greater than the Ge content of Si_xGe_{1-x} by at least 10 atomic percent.

5. The FET device of claim **1**, wherein the Ge content of Si_xGe_{1-x} is greater than the Ge content of the Si layer by at least 10 atomic percent.

6. A FET device, comprising:

a silicon germanium on insulator (SGOI) wafer having an nFET region and a pFET region

wherein the nFET region includes a Si layer located above a Si_xGe_{1-x} layer;

wherein the pFET region includes a Si_zGe_{1-z}, layer located above a Si_yGe_{1-y} layer;

wherein the Si_yGe_{1-y} layer has a germanium (Ge) content equal to or greater than the Si_xGe_{1-x}, layer, and the Si_zGe_{1-z} layer has a Ge content greater than the Si_yGe_{1-y} layer;

wherein the SGOI includes:

a silicon (Si) substrate;

a buried oxide (BOX) layer located above the Si substrate, and

a silicon germanium (SiGe) layer located above the BOX layer;

wherein the Ge content of Si_zGe_{1-z} is greater than the Ge content of Si_yGe_{1-y} by at least 10 atomic percent;

wherein the Ge content of Si_yGe_{1-y} is greater than the Ge content of Si_xGe_{1-x}, by at least 10 atomic percent; and

wherein the Ge content of Si_xGe_{1-x}, is greater than the Ge content of the Si layer by at least 10 atomic percent.

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